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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,151	04/23/2001	Peter A. Miller	017750-606	1629

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Patrick C. Keane  
BURNS, DOANE, SWECKER & MATHIS, L.L.P.  
P.O. Box 1404  
Alexandria, VA 22313-1404

EXAMINER
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PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/839,151

Applicant(s)

MILLER, PETER A.

Examiner

Ishwar (I. B.) Patel

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 10 and 11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 April 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
  - I. Claims 1-9, drawn to a via for use in a printed circuit board, classified in class 174, subclass 261.
  - II. Claims 10-11, drawn to a method of electrically interconnecting multiple layers on a printed circuit board, classified in class 29, subclass 852.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as second interconnect connected to layers forming the signal reference is not required in the product.
3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

***Drawings***

4. The drawings are objected to because figure 1 is improperly crosshatched. All of the parts shown in section, and only those parts, must be crosshatched. The cross hatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

5. Claims 4, 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 4, it is not clear what is meant by "second interconnect is operatively connected to at least two layers of the printed circuit board." It is not clear whether the interconnect is physically connected or is located adjacent to the layers but not connected. The examiner considered the interconnect physically connected with the layers.

Regarding claim 5, the applicant is claiming that a series ground inductance present in the signal return path is essentially cancelled and in claim 6, the applicant is claiming the signal return path has a voltage drop that approaches zero, however these

are all functional limitation and are not adding any structural limitations. The claim in dependent form should contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Yuichi et al., Japanese Patent JP404062894A, hereafter Yuichi.

Regarding claims 1, 5 and 6, Yuichi disclose a via for use in a printed circuit board having a circuit, the via comprising:

a first interconnect (through hole with copper plating 1, see figure 1); and  
a second interconnect located about at least a portion of the first interconnect (hole with plating layer 2, see figure 1),

the second interconnect being coaxial with the first interconnect and inductively coupled with the first interconnect (both the holes with copper plating are co-axial and separated by an insulator, which are inherently inductively coupled),

the second interconnect being connected to ground of the circuit (hole with plating layer 2 connected with copper foil 5 for ground circuit, see figure 1).

Regarding claim 2, Yuichi further discloses first and second interconnects are substantially concentric, see figure 1.

Regarding claim 3, Yuichi further discloses first and second interconnects are cylinders in a single via hole, see figure 1.

Regarding claim 4, Yuichi further discloses the second interconnect connected to layers on both the sides of the interconnect, see figure 1.

Regarding claim 7, Yuichi further discloses the via structure is a part of the single circuit board.

Regarding claim 9, though Yuichi described only one via hole structure, it is a multiplayer circuit board and multiplayer circuit boards inherently comprise more than one via holes depending upon the specific requirement.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yuichi as applied to claims 1-7 and 9 above, and further in view of Duffy et al., US Patent 5,876,842, hereafter Duffy.

Regarding claim 8, the applicant is claiming a circuit board with two or more printed circuit board. Though Yuichi is disclosing only single circuit board, circuit boards made up on multiple circuit board is known in the art and the teaching as disclosed by Yuichi can be used for the circuit board made up of the multiple circuit boards to have the increased wiring density and resultant increased component density. Duffy discloses one such modular structure made up of more than one module circuit boards. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made use the teaching of Yuichi in a circuit board made up of multiple circuit modules as disclosed by Duffy in order to increase the wiring density and the resultant component density.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Suppelsa et al., Breitling et al., Fasano et al., Azzaro et al., Sachdev et al., Reed, Peter et al., Endoh et al., Takahiro and Isatake disclose the structure similar to applicant's claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp  
September 20, 2002

*Robert W. Palmer* 9-23-02  
ROBERT W. PALMER  
PATENT EXAMINER